The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. - 5. (Cancelled)

6. (New) A semiconductor device test apparatus to perform a high voltage test of a device under test (DUT), comprising:

a plurality of source measurement units (SMUs);

a plurality of SMU connectors, each SMU connector electrically connected to a corresponding separate one of the plurality of SMUs;

a tester housing partially enclosing the plurality of SMUs and the plurality of SMU connectors; and

a test fixture, the test fixture configured to be connected to the tester housing such that, in a closed state, the test fixture and the tester housing completely enclose the plurality of SMUs and the plurality of SMU connectors, wherein the test fixture includes

a socket configured to receive pins of the DUT,

a plurality of test fixture connectors, each test fixture connector corresponding to a separate pin of the DUT and configured to, via the socket and when connected by a cable to a corresponding separate one of the plurality of SMU connectors, provide a forcing signal from that test fixture connector to that separate pin of the DUT, receive a sensing signal from that separate pin of the DUT at that test fixture connector, and maintain a guard signal at that separate pin of the DUT at a same electrical potential as the forcing signal.

7. (New) The test apparatus of claim 6, wherein:

the test fixture includes a printed circuit board comprising a plurality of groups of traces, each group of traces corresponding to a separate one of the test fixture connectors and to a separate pin of the DUT and including at least one trace via which the forcing signal is provided from that separate one of the test fixture connectors to that separate pin of the DUT, at least one trace via which the sensing signal is received by that separate one of the test fixture connectors from that separate pin of the DUT, and at least one trace via which the guard signal fully encircles that separate pin of the DUT at a same electrical potential as the forcing signal.

8. (New) The test apparatus of claim 6, wherein:

each test fixture connector includes an internal connection configured such that, only when the cable corresponding to that test fixture connector is fully received to that connector, an outer metallic enclosure surrounding the plurality of wires of the cable is electrically connected to the at least one of the plurality of wires of the cable configured to carry the guard signal.

9. (New) The test apparatus of claim 6, wherein:

the SMU connectors and the test connectors are each configured to receive a min-USB cable.

10. (New) The test apparatus of claim 6, further comprising:

a dedicated DUT cover configured to cover the DUT.

11. (New) A semiconductor device test apparatus to perform a high voltage test of a device under test (DUT), comprising:

a plurality of source measurement units (SMUs);

a plurality of cables, each cable electrically connected to a separate one of the plurality of SMUs;

a tester housing partially enclosing the plurality of SMUs; and

a test fixture, the test fixture configured to be connected to the tester housing such that, in a closed state, the test fixture and the tester housing completely enclose the plurality of SMUs, wherein the test fixture includes

a socket configured to receive pins of the DUT,

a plurality of test fixture connectors, each test fixture connector corresponding to a separate pin of the DUT and configured to, via the socket and when connected by the cable corresponding to a separate one of the plurality of SMUs, provide a forcing signal from that test fixture connector to that separate pin of the DUT, receive a sensing signal from that separate pin of the DUT at that test fixture connector, and maintain a guard signal at that separate pin of the DUT at a same electrical potential as the forcing signal.

12. (New) The test apparatus of claim 11, wherein:

the test fixture includes a printed circuit board comprising a plurality of groups of traces, each group of traces corresponding to a separate one of the test fixture connectors and to a

separate pin of the DUT and including at least one trace via which the forcing signal is provided from that separate one of the test fixture connectors to that separate pin of the DUT, at least one trace via which the sensing signal is received by that separate one of the test fixture connectors from that separate pin of the DUT, and at least one trace via which the guard signal fully encircles that separate pin of the DUT at a same electrical potential as the forcing signal.

13. (New) The test apparatus of claim 11, wherein:

each test fixture connector includes an internal connection configured such that, only when the cable corresponding to that test fixture connector is fully received to that connector, an outer metallic enclosure surrounding the plurality of wires of the cable is electrically connected to the at least one of the plurality of wires of the cable configured to carry the guard signal.

14. (New) The test apparatus of claim 11, wherein:

each cable is a mini-USB cable separately connected to a corresponding SMU via an SMU connector; and

the test connectors are each configured to receive a corresponding one of the min-USB cables.

15. (New) The test apparatus of claim 11, further comprising:

a dedicated DUT cover configured to cover the DUT.